Remarks

Entry of this amendment, reconsideration of the application, and allowance of all claims are respectfully requested. Upon entrance of this amendment, claims 1-35 will be pending.

In accordance with 37 C.F.R. 1.121(c)(1)(ii), a marked-up version of the amended claims is provided on one or more pages separate from the amendment. These pages are appended at the end of the Response.

By this paper, applicants seek to amend claims 1, 2, 9, 16 17 & 27 and add new claims 32-35 to more particularly point out and distinctly claim certain features of applicants' invention. These amendments to the claims constitute a bona fide attempt by the applicants to advance prosecution of this application and obtain allowance of certain claims and are in no way meant to acquiesce to the substance of the Examiner's rejection. It is believed that the amendments to the claims place the claims in condition for allowance and/or in better form for consideration on appeal. These amendments were not made earlier because the amendments are provided by way of further explanation in response to the Examiner's comments contained at paragraph 5, pages 5-8 of the Office Action.

In the Office Action, claims 1-6 and 16-19 were rejected under 35 U.S.C. 102(e) as being anticipated by Greenfield et al (U.S. Patent No. 5,760,836), while claims

7-15 and 20-31 were rejected under 35 U.S.C. 103(a) as being unpatentable over Greenfield et al further in view of Choe et al (U.S. Patent No. 6,094.696). Applicants respectfully traverse these rejections and request reconsideration.

As is well known, there is no anticipation of a claim unless (1) all the same elements are (2) found in exactly the same situation and (3) are united in the same way to (4) perform the identical function. In this case, the encoding techniques of Greenfield et al clearly do not have the same elements, nor are they capable of being readily modified to include the same elements, as that recited by applicants in independent claims 1 & 16.

Applicants recite in these independent claims a technique for encoding a digital video image stream in an encoder. The technique includes feeding back to <u>hardware logic within</u> the encoder an external buffer read signal from a host and incrementing an on-chip counter of the hardware logic each time that the external buffer is read, and counting therefrom the number of bits read by a host (R). The technique further includes determining the number of bits encoded and written into an external buffer (E), and in hardware logic of the encoder subtracting from a number of bits encoded (E) the number of bits read by the host (R) to continuously obtain in real time the fullness of an external buffer (BF). The technique further includes providing, from the hardware logic of the encoder to the host, a <u>dynamic</u> buffer level indicator <u>in real time</u> indicative of the fullness of the external buffer (BF).

Dependent claims 32-35 further recite that the continuous updating comprises obtaining the real time fullness of the external buffer (BF) every cycle of the encoder. Support for this amendment can be found at page 16, lines 17-23, and page 19, lines 1-7 of the specification.

To restate, the present invention employs hardware to continuously monitor the real time fullness of the external buffer and provide in real time a dynamic buffer level indicator indicative of the fullness of the external buffer. This dynamic buffer level indicator assists the host's application and the control of reading compressed data from the external buffer coupled to the encoder. The buffer level indicator is <u>dynamic</u> in that the indicator is adjusted based on continuous real time monitoring of the external buffer. (See page 4, lines 26-33).

In support of the anticipation rejection, the Office Action alleges the teachings at columns 5-7 of Greenfield et al as reciting this aspect of applicants invention. This characterization of the teachings of Greenfield et al is respectfully traversed. In support of this traversal and the following comments, applicants wish to note the significant overlapping in inventorship between the present application and the inventors of the Greenfield et al patent. Applicants are well aware of the teachings and capabilities of the system described in Greenfield et al and note the following differences between that system and the present technique.

Applicants respectfully submit that a careful reading of Greenfield et al fails to uncover any teaching, suggestion or implication that the processing or logic described therein comprises a dynamic buffer level indicator that is provided in real time as recited by applicants herein. In fact, Greenfield et al specifically describes a non-real time buffer level indicator. In Greenfield et al the buffer level indicator is provided dependent upon how often the processor updates the indicator. The hardware described in Greenfield et al would be incapable of supporting any real time application. Column 6, lines 18-29 specifically state that the microcode reads the register and compares it with the buffer fullness in bytes (BF/8). This means that the processor is doing the updating of the buffer level indicator and that the buffer level signal is not returned on a real time basis. As one example, in the Greenfield et al system, a buffer level indicator would be returned approximately once per picture frame.

As noted at page 14 & 15 of applicants' specification, the disadvantage of the above-summarized approach (i.e., the Greenfield et al approach) is that it is implemented in microcode, and therefore, buffer fullness in not constantly monitored. Without a real time view of the fullness of the buffer, the host processor must wait until the microcode goes in, polls the on-chip register and calculates the fullness of the FIFO. This creates a latency issue which produces an inherent inaccuracy in the FIFO fullness reading.

The present invention solves this problem by implementing FIFO monitoring and a dynamic FIFO buffer level indicator in hardware logic inside the digital video encoder for interfacing, for example, to an industry standard FIFO buffer or cascaded FIFO buffers. Thus, applicants attain the recited dynamic buffer level indicator in real time through the use of a hardware implementation. Clearly, Greenfield et al describes a microcode implementation, which, based on the processing described therein, comprises a non-real time implementation. **This is understood by one skilled in the art through the use of a non-real time counter to monitor the amount of data written to the FIFOs in Greenfield et al (see column 6, lines 10-11), and through the use of a non-real time sampling of this counter by the microcode.**

Responsive to the Examiner's comments contained at page 6, lines 7-16 of the Office Action, applicants note that column 1, lines 37-49 and column 5, lines 24-30 each discuss a real time encoder. However, neither of these columns teaches, suggests or implies a real time, continuous monitoring of external buffer fullness as recited in the independent claims presented herewith. Real time encoding is different from and independent of applicants' recited real time monitoring of external buffer fullness. As noted above, the monitoring of external buffer fullness in Greenfield et al. is necessarily non-real time based upon the teachings set forth therein. In fact, the present invention arose from applicants' identifying of the deficiency of the Greenfield et al. teachings in this

respect. The formulas set forth in Greenfield et al. clearly indicate to one skilled in the art that the processor determination of buffer level fullness described therein is a non-real time calculation. To further recite the difference, applicants submit claims 32-35 herewith wherein the real time fullness of the external buffer is determined every cycle of the encoder, i.e., every machine cycle. This is distinct from any teaching, suggestion or implication in Greenfield et al.

In view of the above, applicants respectfully submit that there are clear differences between the encoding technique recited in claims 1 & 16 and the teachings, suggestions or implications in Greenfield et al. Therefore, applicants request withdrawal of the anticipation rejection and allowance of independent claims 1 & 16, as well as the claims which depend therefrom.

As noted, claims 7-15 and 20-31 were rejected under 35 U.S.C. 103(e) as being unpatentable over Greenfield et al further in view of Choe et al. This rejection is respectfully traversed.

First, applicants traverse the combination proposed by the Examiner. Absent from the Office Action is any express teaching, suggestion or incentive identified in the art for making the proposed combination. Just as in *Winner International Royalty Corp. v. Wang*, 48 U.S.P.Q. 2d 1139, 1144 (D.C. 1998), wherein the Court overturned a Board finding of obviousness, hindsight is always perfect and it

is insufficient to prove at the time of the claimed invention, the separate elements of the device were present in the known art. "Rather, there must have been some explicit teaching or suggestion in the art to motivate one of even ordinary skill in the art to combine such elements so as to create the same invention." Id. *Winner's* cited authority, *Arkie Loures Inc. v. Gene Larew Tackle Inc.*, 43 U.S.P.Q. 2d 1294, 1297 (Fed. Cir. 1997), similarly holds that:

> It is insufficient to establish obviousness that the separate elements of the invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the elements.

Just as the multiple document rejection was overturned in *Winner*, the multiple document rejection in the instant Office Action involving Greenfield et al and Choe et al should also be withdrawn.

The only justification given for the combination of the documents is the following passage at page 8 of the Office Action:

> ... Therefore, it would have been obvious to one of ordinary skill in the art, having the Greenfield et al and Choe et al references in front of him/her and the general knowledge of flag indicating statuses for a buffer management system, would have had no difficulty in providing the buffer flagging system as taught by Choe et al as part of the buffer management within Figure 5 of Greenfield et al for the

same well known flag identification purposes as claimed.

Applicants respectfully submit that this passage does not identify an adequate teaching, suggestion or incentive in the art itself to combine these references as required by *Winner & Arkie*, but rather simply restate the ultimate result of the combination in a conclusory manner without any underlying reasoning supporting the combination.

In fact, since this rejection simply restates the results of the present invention, it also violates the well known principle that an applicant's own disclosure cannot be used as a reference against him.

The consistent criterion for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the claimed process should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, **not in the applicant's disclosure**. In *re Dow Chemical Co.* 5 U.S.P.Q. 2d 1529, 1531 (Fed. Cir. 1988) (multiple citations omitted). Here, the results of this combination are drawn from Applicants' disclosure, in violation of this principle.

Even assuming, arguendo, that the combination is proper, the combination still fails to teach or suggest certain features of the claimed invention. For example, each independent claim at issue (i.e., claims 9 & 27)

recites a technique wherein hardware logic within the encoder provides to the host in real time a dynamically updated flag. Neither Greenfield et al nor Choe et al provide from an encoder to a host a dynamically updated flag in real time. In fact, applicants note that Choe et al does not even involve an encoding process.

As noted above, a careful reading of Greenfield et al fails to uncover any teaching, suggestion or implication of an encoding technique wherein a dynamic buffer level indicator is provided to a host in real time. Similarly, a careful reading of Choe et al fails to uncover any discussion of an encode process, let alone the provision of a dynamic buffer level indicator in real time from an encoder to a host. In fact, a careful reading of Choe et al fails to uncover any dynamic indicator being provided in real time. Choe et al disclose a data transfer mechanism where a set of buffer_full and buffer_empty flag are implemented for each device. The flags disclosed for Choe et al are not-real time. Once a flag is set it has to be reset by the CPU. This is in contrast with the flags disclosed by applicants which are dynamic, real time indicators. As the data is added to the pre-defined full level the buffer_full flag is asserted in applicants' case. Further as data is removed to below the pre-defined full level, the buffer_full flag is deasserted without any CPU intervention. The flags of Choe et al are used to start data transfer operations. In contrast, the flags recited by applicants do not necessarily initiate data transfer.

Applicants flags are used to regulate the data rate in and out of the FIFOs in a simultaneous and continuous manner.

Applicants respectfully submit that an "obviousness" determination requires an evaluation of whether the prior art taken as a whole would suggest the claimed invention taken as a whole to one of ordinary skill in the art. Since all of the recited elements of applicants independent claims are <u>not</u> disclosed in the various applied patents, the claims taken as a whole cannot be said to be obvious. Applicants respectfully submit that independent claims 9 & 27 would <u>not</u> have been obvious to one of ordinary skill in the art based on the applied patents.

In summary, applicants traverse the obviousness rejection of the independent claims because (1) no express teaching, suggestion or incentive in the art is identified for the combination; (2) the rejection simply restates results of the invention from applicants' specification; (3) even assuming, arguendo, that the combination is proper, the combination still fails to disclose, teach or suggest applicants recited concept of providing a <u>dynamic</u> host buffer level indicator from an encoder to a host <u>in real time</u>; and (4) Greenfield et al's and Choe et al's teachings are insufficient to support a position that any indicators described therein comprise dynamic indicators provided in real time.

Withdrawal of the rejection to independent claims 9 & 27 is therefore requested. The dependent claims are

believed allowable for the same reasons as the independent claims, as well as for their own additional characterizations.

In view of the above Amendments and Remarks, applicants respectfully request allowance of all claims pending herein. Should the Examiner wish to discuss the case with applicants' attorney, please contact applicants' attorney at the below listed number.

Respectfully submitted,

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Marked-Up Version of Claims

1. (Twice Amended) In a method of encoding a digital video image stream in an encoder, comprising spatial compression of still images in the digital video image stream and temporal compression between the still images, wherein the spatial compression is carried out by converting a time domain image of a macroblock to a frequency domain image of the macroblock, taking a discrete cosine transform of the frequency domain image, transforming the discrete cosine transformed macroblock image by a quantization factor, and run length encoding the quantized discrete cosine transformed macroblock image, wherein the temporal compression is carried out by reconstructing the quantized, discrete cosine transformed image of the macroblock, searching for a best match macroblock, and constructing a motion vector therebetween, to thereby form a bitstream comprising run length encoded, quantized, discrete cosine transformed macroblocks and motion vectors, and passing the bitstream to and through an external buffer to a transmission medium, the improvement comprising feeding back to <u>hardware logic within</u> the encoder an external buffer read signal from a host and incrementing an on-chip counter <u>of the hardware logic</u> each time that the external buffer is read and calculating therefrom the number of bits read by a host (R), and determining the number of bits encoded and written into an external buffer (E), and in the <u>hardware logic of the</u> encoder subtracting from a number of bits encoded (E) the number of bits read by the host (R) to <u>continuously obtain</u> [give] the <u>real time</u> fullness of an

external buffer (BF), and providing, from the hardware logic within the encoder to the host, a dynamic buffer level indicator in real time indicative of the fullness of the external buffer (BF).

2. (Twice Amended) The method of claim 1, wherein said providing the host with said dynamic buffer level indicator comprises continuously comparing the real time fullness of the external buffer (BF) with a buffer threshold (BT) defined by said host and providing a high-level indicator when a buffer fullness (BF) is greater than the buffer threshold (BT), and a low-level indicator when the buffer threshold (BT) is greater than the buffer fullness (BF).

9. (Twice Amended) In a method of encoding a digital video image stream in an encoder, comprising spatial compression of still images in the digital video image stream and temporal compression between the still images, wherein the spatial compression is carried out by converting a time domain image of a macroblock to a frequency domain image of the macroblock, taking a discrete cosine transform of the frequency domain image, transforming the discrete cosine transformed macroblock image by a quantization factor, and run length encoding the quantized discrete cosine transformed macroblock image, wherein the temporal compression is carried out by reconstructing the quantized, discrete cosine transformed image of the macroblock, searching for a best match macroblock, and constructing a motion vector therebetween, to thereby form a bitstream

comprising run length encoded, quantized, discrete cosine transformed macroblocks and motion vectors, and passing the bitstream to and through an external buffer to a transmission medium, the improvement comprising feeding back to hardware logic within the encoder an external read signal from a host and incrementing an on-chip counter of the hardware logic each time that the external buffer is read and calculating therefrom the number of bits read by a host (R), and determining the number of bits encoded and written into an external buffer (E), and in the hardware logic of the encoder subtracting from a number of bits encoded (E) the number of bits read by the host (R) to continuously obtain [give] the real time fullness of an external buffer (BF), and providing, from the hardware logic within the encoder to the host, in real time a dynamically updated flag comprising at least one of a BUFFER_EMPTY flag, a BUFFER_ALMOST_FULL flag and a BUFFER_FULL flag.

16. (Twice Amended) An encoder for encoding a digital video image stream in the encoder, comprising means for spatial compression of still images in the digital video image stream and means for temporal compression between the still images, wherein the means for spatial compression comprises means for converting a time domain image of a macroblock to a frequency domain image of the macroblock, means for taking a discrete cosine transform of the frequency domain image, means for transforming the discrete cosine transformed macroblock image by a quantization factor, and means for run length encoding the quantized discrete cosine transformed macroblock image, wherein the

means for temporal compression comprises means for reconstructing the quantized, discrete cosine transformed image of the macroblock, means for searching for a best match macroblock, and means for constructing a motion vector therebetween, said encoder for encoding a digital video image stream thereby forming a bitstream comprising run length encoded, quantized, discrete cosine transform macroblocks and motion vectors and passing the bitstream to and through an external buffer to a transmission medium, the improvement comprising means for feeding back to <u>hardware logic within</u> the encoder an external read signal from a host, and [logic in the encoder] for incrementing an on-chip counter <u>of the hardware logic</u> each time that the external buffer is read and calculating therefrom the number of bits read by a host (R), said <u>hardware</u> logic in the encoder being further adapted to monitor a number of bits encoded (E) and written into the external buffer and subtract from the number of bits encoded (E) the number of bits read by the host (R) to <u>continuously</u> obtain the <u>real time</u> fullness of an external buffer (BF), and wherein said <u>hardware</u> logic in the encoder is further adapted to provide the host with a dynamic buffer level indicator in real time indicative of the fullness of the external buffer (BF).

17. (Twice Amended) The encoder of claim 16, wherein said logic adapted to provide the host with a dynamic buffer level indicator comprises logic adapted to <u>continuously</u> compare the <u>real time</u> fullness of the external buffer (BF) with a buffer threshold (BT) defined by said host and to provide a high-level indicator when a buffer fullness (BF)

is greater than the buffer threshold (BT), and a low-level indicator when the buffer threshold (BT) is greater than the buffer fullness (BF).

27. (Twice Amended) An encoder for encoding a digital video image stream in the encoder, comprising means for spatial compression of still images in the digital video image stream and means for temporal compression between the still images, wherein the means for spatial compression comprises means for converting a time domain image of a macroblock to a frequency domain image of the macroblock, means for taking a discrete cosine transform of the frequency domain image, means for transforming the discrete cosine transformed macroblock image by a quantization factor, and means for run length encoding the quantized discrete cosine transformed macroblock image, wherein the means for temporal compression comprises means for reconstructing the quantized, discrete cosine transformed image of the macroblock, means for searching for a best match macroblock, and means for constructing a motion vector therebetween, said means for encoding a digital video image stream thereby forming a bitstream comprising run length encoded, quantized, discrete cosine transform macroblocks and motion vectors and passing the bitstream to and through an external buffer to a transmission medium, the improvement comprising means for feeding back to <u>hardware logic within</u> the encoder an external read signal from a host, and [on-chip logic in the encoder] for incrementing an on-chip counter <u>of the hardware logic</u> each time the external buffer is read and calculating therefrom the number of bits read by

a host (R), said <u>hardware</u> logic in the encoder being further adapted to monitor a number of bits encoded (E) and written into the external buffer and subtract from the number of bits encoded (E) the number of bits read by the host (R) to <u>continuously</u> obtain the <u>real time</u> fullness of an external buffer (BF), and wherein said <u>hardware</u> logic in the encoder is further adapted to provide the host in real time with dynamically updated flags comprising a BUFFER_EMPTY flag, a BUFFER_ALMOST_FULL flag and a BUFFER_FULL flag.

32. (New) <u>The method of claim 1, wherein the continuously obtaining comprises obtaining the real time fullness of the external buffer (BF) every cycle of the encoder.</u>

33. (New) <u>The method of claim 9, wherein the continuously obtaining comprises obtaining the real time fullness of the external buffer (BF) every cycle of the encoder.</u>

34. (New) <u>The encoder of claim 16, wherein the hardware logic continuously obtains the real time fullness of the external buffer (BF) every cycle of the encoder.</u>

35. (New) <u>The encoder of claim 27, wherein the hardware logic continuously obtains the real time fullness of the external buffer (BF) every cycle of the encoder.</u>